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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MAGEE, THOMAS J	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 11/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,015	RUDECK ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. The amendment changing the wording of Claim 17 is acknowledged and is acceptable. The objection is herewith removed.

Claim Rejections – 35 U.S.C. 112

2. Claim rejections under 35 U.S.C., first paragraph, have been removed.

3. The amendment changing the wording of Claim 18 is acknowledged and is acceptable. The rejection under 35 U.S.C. 112, second paragraph, is herewith removed.

Claim Rejections – 35 U.S.C. 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 – 4, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakajima et al. (US 5,397,724).

6. Regarding Claims 1 and 19, Nakajima et al. disclose a semiconductor device comprising a substrate (2) (Figure 3E), a drain (24a) formed in the substrate, a self aligned source region (24b) (Col. 3, lines 66 – 68) formed in the substrate, a first oxide layer deposited over the

substrate and stretching from drain to source (6), a first polysilicon layer (8) deposited over the first oxide layer, a second oxide layer (10) deposited over the first polysilicon layer (8), said self aligned source extending to a point inward of an edge of the first polysilicon layer, and a second polysilicon layer (12) deposited over the second oxide layer(10, and a phosphorous-doped oxide (30) along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer.

7. Regarding Claim 2, Nakajima et al. do not explicitly disclose that the first oxide layer (6) is a tunnel oxide layer, however, the device is disclosed to be an EPROM with floating gate and control gate (Col. 3, lines 32 – 43), wherein it is implicit that the first thin insulating layer is a tunnel oxide.

8. Regarding Claim 3, Nakajima et al. disclose that the second oxide layer (10) is an oxide-nitride-oxide (ONO) layer (Col. 3, lines 45 – 48).

9. Regarding Claim 4, Nakajima et al. disclose that the first polysilicon layer (8) is a floating gate (Col. 3, line 37).

10. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al., as applied to Claims 1 – 4, and further in view of Bergemont et al. (US 5,856,222).

11. Regarding Claim 5, Nakajima et al. do not explicitly disclose the presence of word-lines formed from the second polysilicon layer. Bergemont et al. disclose (Figure 5B)

that the second polysilicon layer (control gate) forms a wordline.
It would have then been obvious to combine Bergemont et al. with Nakajima et al., to form an interconnected working device.

12. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al. in view of Rodder (US 6,329,225 B1).

13. Regarding Claim 6, Nakajima et al. disclose a semiconductor device after re-oxidation, wherein the device comprises a substrate (2) (Figure 3E), a drain (24a) formed in the substrate, a self aligned source region (24b) (Col. 3, lines 66 – 68) formed in the substrate, a first oxide layer deposited over the substrate and stretching from drain to source (6), a first polysilicon layer (8) deposited over the first oxide layer, a second oxide layer (10) deposited over the first polysilicon layer (8) and a second polysilicon layer (12) deposited over the second oxide layer (10), and a phosphorous-doped oxide (30) along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer.

Nakajima et al. do not disclose the re-oxidation profile. Rodder discloses (Col.5, lines 43 - 46) (Figure 2A) the reoxidation profile (layer 128) over the semiconductor device surface and having a height and width after formation. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Rodder with Nakajima et al. to ascertain an oxide layer profile subsequent to oxidation exposure.

14. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al.

in view of Rodder, as applied to Claim 6, and further in view of Sobek et al. (US 6,268,624 B1).

15.Regarding Claim 7, Nakajima et al. do not disclose the structure developed at the polysilicon/oxide interfaces subsequent to reoxidation or the dependency on properties of the phosphorous-doped oxide (PSG).

Sobek et al. disclose (Col. 2, lines 1 - 17) (Figure 1) that the re-oxidation process, results in inter layer encroachment and the development of "cuspate" structure characterized by a "height" and a "width." Sobek discloses that the indiffusion of oxygen into the edges of the oxide produces the cuspate structure (Col. 2, lines 7 – 9). Further Sobek et al. disclose that dielectrics at the lateral edges of the structure (Figure 3) eliminate the development of "cuspate" structure (Figure 1) characterized by a width or distance from a side edge to a vertical edge during reoxidation (Col. 4, lines 31 -36) (Abstract) and the "width" is relatively reduced compared to that without a deposited layer at the edges. Hence, the reduction in oxygen diffusion reduces cuspate structure. In like fashion, Applicant admits (p.10, Specification, lines 6 – 8) that the "phosphorous doped oxide acts as a barrier against the diffusion of oxygen during reoxidation." Therefore, the oxide containing phosphorous will further suppress oxgen diffusion and the width of the reoxidation profile is less than that without the phosphorous doped oxide. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Sobek et al. with Nakajima et al. to obtain a reduced reoxidation width and cuspate profile.

16. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Riedel (US

6,732,241 B2) in view of Nakajima et al. and Sobek et al.

17. Regarding Claim 13, Riedel discloses a computer (or data processing system) (100) (Col. 3, line 56 through Col. 4, line 10) (Figure 1) comprising a processor (102), a system bus (106) and a flash memory device (114) coupled to the system bus (106). Riedel does not disclose the structure of the flash memory device. Nakajima et al. disclose a memory device comprising a substrate (2) (Figure 3E), a drain (24a) formed in the substrate, a self aligned source region (24b) (Col. 3, lines 66 – 68) formed in the substrate, a first oxide layer deposited over the substrate and stretching from drain to source (6), a first polysilicon layer (8) deposited over the first oxide layer, a second oxide layer (10) deposited over the first polysilicon layer (8) and a second polysilicon layer (12) deposited over the second oxide layer (10, and a phosphorous-doped oxide (30) along substantially vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer and the second polysilicon layer.

Neither Riedel nor Nakajima et al. disclose the reoxidation profile formed over surfaces of the semiconductor device and having a height and width. Sobek et al. disclose (Col. 2, lines 1 – 17) (Figure 1) that the re-oxidation process, results in inter layer encroachment and the development of "cuspate" structure characterized by a "height" and a "width." Sobek discloses that the indiffusion of oxygen into the edges of the oxide produces the cuspate structure (Col. 2, lines 7 – 9). Hence, a reduction in oxygen diffusion reduces cuspate structure. In like fashion, Applicant admits (p.10, Specification, lines 6 – 8) that the "phosphorous doped oxide acts as a barrier against the diffusion of oxygen during reoxidation." Therefore, the oxide

containing phosphorous will further suppress oxgen diffusion and a reduced height and width of the reoxidation profile is present. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Sobek et al. with Nakajima et al. to obtain a reduced reoxidation and cuspate profile.

18. Claims 14 - 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al. in view of Wolf et al. ("Silicon Processing for the VLSI Era, Vol. 1 – Process Technology," Lattice Press, Sunset Beach, CA (1986) p. 286) and Rodder.

19. Regarding Claim 14, Nakajima et al. disclose a horizontal layer (12) (Figure 3E), wherein the layer is implanted to a first doping concentration (Col. 5, lines 21 – 35), a vertical layer (implanted) perpendicular and coupled to the horizontal layer (edge of layer 12), produced by the lateral or angular spread of the ion implant beam (Wolf et al., Figure 3, p.286), wherein the doping concentration is lower than said first doping concentration, and a vertical phospho-ous doped oxide layer (30) provided on the vertical layer, the vertical phosphorous doped oxide layer having a third doping concentration.

Nakajima et al. do not disclose a self aligned source having a resistance less than a self aligned source without the vertical phosphorous doped oxide layer and a trench depth deeper than the self aligned source without the vertical phosphorous doped oxide layer. Rodder discloses that the sidewalls (142) (Figure 2C) define a limited implant area (144) for source/drain implants, allowing the implants to be deeply diffused without damaging the channels, resulting in increased trench depths and lower resistance (Col. 6, lines 6 – 16), It would have been

obvious to one of ordinary skill in the art at the time of the invention to combine the structure of Nakajima et al. with the phosphorous doped vertical sidewalls and the implant procedure of Rodder to obtain a deeper source region of low resistivity.

20. Regarding Claims 15 and 16, Nakajima et al. do not explicitly disclose that the third and second doping concentrations produce an effective doping concentration equal to the first concentration or that the third concentration is in the range of about 1 to 6 percent. Parameters such as concentration in the art of semiconductor processing are subject to routine experimentation and optimization to achieve the desired device performance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the doping concentrations as claimed to achieve an efficient, operable device.

21. Regarding Claim 17, Nakajima et al. do not disclose that the thickness of the vertical phosphorous doped oxide layer is in the range of about 25 to 500 Angstroms. It would have been obvious to one of ordinary skill in the art at the time of the invention to conduct a series of tests to optimize and to incorporate thicknesses in the claimed range to produce an efficient, operable device.

22. Regarding Claim 18, Nakajima et al. do not disclose the third doping concentration and thickness of the vertical phosphorous doped oxide layer selected to achieve desired characteristics of the flash memory cell, including program rate, ease rate, and data retention. Parameters such as concentration and thickness of layers in the art of semiconductor processing are

subject to routine experimentation and optimization to achieve the desired device performance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the optimized doping concentration and thickness to achieve an efficient, operable device.

23. Claims 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al. in view of Rodder and Sobek et al.

24. Regarding Claims 20 and 21, Nakajima et al. disclose, as discussed for Claims 6 and 7, a semiconductor device after re-oxidation comprising: a substrate, a drain (self aligned) and source (self aligned), a first oxide stretching from drain to source, a first polysilicon layer over the first oxide, said self aligned source extending to a point inward of an edge of the first polysilicon layer, a second oxide deposited over the first polysilicon layer, a second polysilicon layer deposited over the second oxide layer, and a phosphorous doped oxide layer deposited along vertical edges of the first oxide layer, the first polysilicon layer, the second oxide layer, and the second polysilicon layer.
Nakajima et al. do not disclose the structure developed at the polysilicon/oxide interfaces subsequent to reoxidation or the dependency on properties of the phosphorous-doped oxide (PSG). Sobek et al. disclose (Col. 2, lines 1 - 17) (Figure 1) that the re-oxidation process, results in inter layer encroachment and the development of "cuspate" structure characterized by a "height" and a "width," wherein the width is defined as a horizontal distance from a side edge of the first polysilicon layer to a vertical edge of the tunnel oxide layer where the first

oxide layer starts to get thicker than the first thickness, and the height is defined by a vertical distance from a top surface of the self aligned source to a bottom edge of the first polysilicon layer. Sobek discloses that the indiffusion of oxygen into the edges of the oxide produces the cuspate structure (Col. 2, lines 7 – 9). Further Sobek et al. disclose that dielectrics at the lateral edges of the structure (Figure 3) eliminate or reduce the development of "cuspate" structure (Figure 1) characterized by a width or distance from a side edge to a vertical edge during reoxidation (Col. 4, lines 31 -36) (Abstract) and the "width" and height are relatively reduced compared to that without a deposited layer at the edges. Hence, the reduction in oxygen diffusion reduces cuspate structure. In like fashion, Applicant admits (p.10, Specification, lines 6 – 8) that the "phosphorous doped oxide acts as a barrier against the diffusion of oxygen during reoxidation." Therefore, the oxide containing phosphorous will further suppress oxgen diffusion and the width and height of the reoxidation profile is less than that without the phosphorous doped oxide. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Sobek et al. with Nakajima et al. to obtain a reduced reoxidation width and cuspate profile.

Response to Arguments

25. Arguments of Applicant with respect to claim rejections have been carefully considered by Examiner, but these are moot in terms of the new ground(s) of rejection.

Conclusions

26. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(703) 305**

5396. The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(703) 308-1690.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

Thomas Magee
November 16, 2004

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